

MEASURE-CONTROLLED CIRCUIT WITH FREQUENCY CONTROL

This application is a Continuation of U.S. Application No. 10/147,657, filed May 16, 2002 which is incorporated herein by reference.

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Field

The present invention relates generally to integrated circuits, and in particular to delay locked circuits.

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Background

Delay locked circuits reside in many integrated circuits for delaying an external signal to obtain an internal signal. The delay locked circuit automatically tracks the external and internal signals to keep them synchronized. The internal signal usually serves as a reference signal for the integrated circuits instead of the external signal because the internal signal matches internal operating conditions of the integrated circuits, such as process, voltage, and temperature, better than the external signal does.

One type of delay locked circuit measures a timing of the external signal in every cycle (period) of the external signal. Based on the measurement, the delay locked circuit adjusts the delay applied to the external signal to keep the external and internal signals synchronized.

In many cases, the operating conditions of the integrated circuit remain unchanged for a time substantially greater than the cycle time of the external signal. Therefore, measuring the external signal to adjust the delay in every cycle time of the external signal wastes power.

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Summary of the Invention

Various embodiments of the invention provide circuits and methods to operate a delay locked circuit more efficiently.

In one aspect, the delay locked circuit includes a measuring unit for obtaining a reference time based on a cycle time of an external signal during a measurement on a

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first path of the external signal. The delay locked circuit uses the reference time to acquire a measured delay. An adjusting unit adjusts a delay on a second path of the external signal based on the measured delay. The delay locked circuit also includes an interval controller for controlling a time interval between one measurement and the next
5 measurement.

In another aspect, a method of processing signals includes propagating an external signal on a measuring path. A measurement is performed on the measuring path to acquire a measured delay. The method also propagates the external signal on an output path to produce an internal signal. A correction delay based on the measured
10 delay is applied to the output path. The method further performs another measurement at a time interval unequal to the cycle time of the external signal.

Brief Description of the Drawings

Figure 1 shows a delay locked circuit according to an embodiment of the
15 invention.

Figure 2 shows an example of a timing diagram for Figure 1.

Figure 3 shows more detail of the delay locked circuit of Figure 1.

Figure 4 shows another embodiment of correction delay line of Figure 3.

Figure 5 shows a delay locked circuit having counters according to an
20 embodiment of the invention.

Figure 6 shows a delay locked circuit having charge circuits according to an embodiment of the invention.

Figure 7 shows an embodiment of an interval controller of Figure 1.

Figure 8 shows a timing diagram for Figure 7.

25 Figure 9 shows a memory device according to an embodiment of the invention.

Figure 10 shows a system according to an embodiment of the invention.

Description of embodiments

The following description and the drawings illustrate specific embodiments of the invention sufficiently to enable those skilled in the art to practice it. Other embodiments may incorporate structural, logical, electrical, process, and other changes.

5 Examples merely typify possible variations. Portions and features of some embodiments may be included in or substituted for those of others. The scope of the invention encompasses the full ambit of the claims and all available equivalents.

Figure 1 shows a delay locked circuit according to an embodiment of the invention. Delay locked circuit 100 includes an external node 102 for receiving an
10 external signal XCLK and an internal node 104 for outputting and internal signal INTCLK. The XCLK signal propagates on two paths, a measuring path 106 and an output path 108. Measuring path 106 has a measuring unit 110 for periodically performing a measurement to measure a timing of the XCLK signal. Output path 108 has an adjusting unit 112 for periodically adjusting a delay of output path 108 based on
15 the measurement.

Measuring unit 110 includes a delay model circuit 114 and a converter 116. During each measurement, delay model circuit 114 delays a signal by an amount of time T_{DL} . Converter 116 converts a reference time T_{REF} into a measured delay. T_{REF} is a measurement of time, whereas the measured delay is a quantity other than time but
20 depending on T_{REF} .

Delay model circuit 114 is modeled after a combination of an input buffer 118 and an output buffer 120 so that a time delay of delay model circuit 114, T_{DL} , equals the sum of a time delay of input buffer 118, T_{IN} , and a time delay of output buffer 120, T_{OUT} , ($T_{DL}=T_{IN} + T_{OUT}$).

25 The XCLK signal has a cycle time T_{CK} . The sum of T_{DL} and T_{REF} equals one or more cycle times of the XCLK signal. $MT_{CK} = T_{DL} + T_{REF}$ or $T_{REF} = MT_{CK} - T_{DL}$, where M is an integer equal to or greater than one.

Adjusting unit 112 includes a correction delay line 122 for applying a correction delay to the output path 108 based on the measured delay. The correction delay and the measured delay have an equal delay quantity.

On output path 108, the XCLK signal propagates from node 102 through input
5 buffer 118, the correction delay line 122, and output buffer 120 to become the INTCLK signal. The INTCLK signal and the XCLK signal are synchronized because the correction delay equals the measured delay. As shown in Figure 1, $MT_{CK} = T_{DL} + T_{REF}$ where $T_{DL} = T_{IN} + T_{OUT}$, and the correction delay corresponds to T_{REF} . Thus, $MT_{CK} = T_{IN} + T_{OUT} + T_{REF}$. On output path 108, $T_{IN} + T_{OUT} + T_{REF}$ is the delay applied to the XCLK
10 signal when it travels from node 102 to node 104 to become the INTCLK signal. Hence, the INTCLK signal is the XCLK signal delayed by $T_{IN} + T_{OUT} + T_{REF}$. Since $MT_{CK} = T_{IN} + T_{OUT} + T_{REF}$, the INTCLK signal is the XCLK signal delayed by MT_{CK} .

Delay locked circuit 100 further includes an interval controller 124 connected to measuring unit 110. Interval controller 124 receives an input signal CLKIN and
15 generates a measuring start signal START and a measuring stop signal STOP. The START and STOP signals control a time interval between one measurement and the next measurement and control the duration of each measurement. The START signal starts a measurement and the STOP signal stops the measurement. The START signal is a periodic signal. Interval controller 124 sets the time interval between one
20 measurement and the next measurement to be equal to the cycle time of the START signal. Interval controller 124 sets the duration of each measurement to be one or more cycle times of the XCLK signal and less than the cycle time of the START signal.

Figure 2 shows an example of a timing diagram for Figure 1. D1 and D2 indicate a time delay between the XCLK and INTCLK signals at time T0 and T3,
25 respectively. Interval controller 124 activates the START signal (high) at time T0 to start a measurement and activates the STOP signal at times T1 to stop the measurement. Between these times, measuring unit 110 performs a measurement based on T_{REF} to obtain the measured delay. In Figure 2, the duration of the measurement is one cycle time of the XCLK signal. Therefore, M equals one and T_{REF} equals one T_{CK} minus T_{DL} .

Between times T1 and T2, adjusting unit 112 applies a correction delay to output path 108 based on the measured delay. At time T2, the XCLK and INTCLK signals become synchronized. The process repeats between times T3-T4. At time T3, interval controller 124 activates the START signal again to start a new measurement. The

5 XCLK and INTCLK signals may be out of synchronization at time T3. For example, at time T3, the XCLK and INTCLK signals have a delay D2. Adjusting unit 112 applies another correction delay based on the measured delay obtained by the new measurement.

The time interval between one measurement and the next measurement equals

10 the cycle time of the START signal T_{START} . $T_{START} = NT_{CK}$, where N is greater than one. Thus, T_{START} is greater than T_{CK} . The STOP signal has a cycle time T_{STOP} . In Figure 2, T_{STOP} equals T_{START} . In some embodiments, T_{STOP} is unequal to T_{START} .

The duration of each measurement equals the time interval between the activations of the START and STOP signals. This time interval equals MT_{CK} . In Figure

15 2, M equals one. Therefore, the duration of each measurement equals one T_{CK} . In some embodiments, M is greater than one and less than N. Thus, the duration of each measurement equals more than one T_{CK} .

In Figure 2, since the time interval between one measurement and the next measurement equals T_{START} where T_{START} is greater than T_{CK} , the number of

20 measurements based on T_{START} is less than the number of measurements based on T_{CK} . Therefore, using T_{START} instead of T_{CK} between one measurement and the next measurement saves power.

Figure 3 shows more detail of the delay locked circuit of Figure 1. Converter 116 has a number of measuring delay elements (M) 302.1-302.X connected to a number

25 of storage elements (L) 304.1-304.X. Measuring delay elements 302.1-302.X have output nodes to output signals M1-MX. A control logic 305 determines the contents of storage elements 304.1-304.X to activate one of the select signals S1-SN. Correction delay line 122 having a number of correction delay elements (C) 306.1-306.X, each being controlled by one of the S1-SN signals. The CLKIN signal enters correction delay

line 122 at a variable entry point at any one of the inputs of correction delay elements 306.1-306.X. The CLKIN signal exits the correction delay line 122 at fixed exit point at the output of correction delay elements 306.1. Control logic 305 activates one of the select signals S1-SN to select the entry point.

5 Storage elements 304.1-304.X can be flip flops, latches, registers, or other devices capable of storing a state (level) of a signal. Each of the measuring delay elements and each of correction delay elements delays a signal for an equal amount of delay.

 In a measurement, interval controller 124 activates the START signal at a
10 starting time of the measurement. For example, at starting time T_0 , the START signal is activated and propagates through delay model circuit 114 for a time equal to T_{DL} . At time $T_0 + T_{DL}$, the START signal enters measuring delay elements 302.1 and propagates through a certain number measuring delay elements for a time equal to T_{REF} . For example, the START signal propagates through three measuring delay elements during
15 T_{REF} . At time $T_0 + T_{DL} + T_{REF}$, or after MT_{CK} from T_0 , the STOP signal is activated to enable storage elements 304.1-304.X to latch the M1-MX signals.

 Control logic 305 examines the contents of storage elements 304.1-304.X to determine the last measuring delay elements reached by the START signal when the STOP signal is activated. Based on the contents of storage elements 304.1-304.X,
20 control logic 305 activates one of the S1-SN signals to select the entry point. The CLKIN signal enters the entry point and propagates through a number of correction delay elements equal to the number of measuring delay elements that the START signal propagates through during T_{REF} . The CLKIN signal becomes the INTCLK signal at node 104.

25 In the example where the START signal propagates through three measuring delay elements during T_{REF} , control logic 305 activates the S3 signal to select the entry point at correction delay element 306.3. The CLKIN signal propagates from the entry point to node 104 through three correction delay elements 306.1-306.3. Thus, the measured delay equals three measuring delay elements and the correction delay equals

three correction delay elements. Since each of the measuring delay elements and each of correction delay elements delays a signal for an equal amount of delay, the correction delay equals the measured delay.

Figure 4 shows another embodiment of correction delay line 122 of Figure 3. In Figure 4, the CLKIN signal enters correction delay line 122 at a fixed entry point at correction delay element 306.1. The CLKIN signal exits correction delay line 122 at a variable exit point at any one of the outputs of correction delay elements 306.1-306.X. Control logic activates one of the S1-SN signals to select the exit point. For example, when the S3 signal is activated, the CLKIN signal exits correction delay line 122 at correction delay element 306.3 after propagating through three correction delay elements 306.1-306.3.

Figure 5 shows a delay locked circuit having counters according to an embodiment of the invention. Delay locked circuit 500 has measuring path 106 and output path 108. Measuring path 106 has a measuring counter 502. Output path 108 has a correction counter 504. Measuring path 106 obtains a measured delay while counter 502 counts up during T_{REF} . Output path 108 applies a correction delay equal to the measured delay while correction counter 504 counts down.

During time T_{REF} of a measurement, measuring counter 502 counts up from zero to a counted number. The START signal starts the count. The STOP signal stops the count. The counted number corresponds to the measured delay. Correction counter 504 loads the counted number and counts down from the counted number to zero. Based on the count down by correction counter 504, output path 108 applies a correction delay to the CLKIN signal equal to the measured delay.

Figure 6 shows a delay locked circuit having charge circuits according to an embodiment of the invention. Delay locked circuit 600 has measuring path 106 and output path 108. Measuring path 106 has a measuring charge circuit 602. Output path 108 has a correction charge circuit 604. Measuring path 106 obtains a measured delay while measuring charge circuit 602 charges up during T_{REF} . Output path 108 applies a

correction delay equal to the measured delay while correction charge circuit 604 discharges.

During time T_{REF} of a measurement, measuring charge circuit 602 charges up to a reference charge. The START signal starts the charging process. The STOP signal
5 stops the charging process. The reference charge corresponds to the measured delay. The reference charge is transferred to correction charge circuit 604, which discharges the reference charge. Based on the discharge by correction charge circuit 604, output path 108 applies a correction delay to the CLKIN signal equal to the measured delay.

Figure 7 shows an embodiment of interval controller 124 of Figure 1. Interval
10 controller 124 includes a programmable frequency modifier 710 and a frequency shifter 712. Programmable frequency modifier 710 divides the frequency of the CLKIN signal to generate the START signal. The cycle time of the START signal is greater than the cycle time of the CLKIN signal. Since the CLKIN signal is a delayed version of the XCLK signal, the CLKIN and XCLK signals have an equal cycle time. Therefore, the
15 cycle time of the START signal is also greater than the cycle time of the XCLK signal. Programmable frequency shifter 712 shifts the START signal by one or more cycle time of the XCLK signal.

Programmable frequency modifier 710 includes a plurality of flip flops 714.1-714.n, each having two input nodes CLK and D, and two output nodes Q and Q*. In
20 some embodiments, each of the flip flops 714.1-714.N is a D-Q flip flop. Flip flops 714.1-714.n form a frequency divider that divides the CLKIN signal into a plurality of selectable start signals ST1 through STn. Each succeeding selectable start signal has a cycle time equal to twice the cycle time of the preceding selectable start signal. The STn signal has a cycle time equaled to 2^n times the cycle time of the CLKIN signal,
25 where n is the total number of flip flops 714.1-714.n.

A selector 716 selects one of the ST1-STn signals as the START signal based on a combination of select signals SEL1-SELx. In some embodiments, selector 716 is a n:1 multiplexor.

Programmable frequency shifter 712 includes a plurality of flip flops 718.1-718.m, each having two input nodes CLK and D, and two output nodes Q and Q*. In some embodiments, each of the flip flops 718.1-718.m is a D-Q flip flop. Flip flops 718.1-718.m shift the START signal to provide a plurality of selectable stop signals
5 SP1-SPm. Each succeeding selectable stop signal is shifted by one cycle time of the XCLK signal from the preceding selectable stop signal. The STm signal is shifted by m cycle time of the XCLK signal from the SP1 signal, where m is the total number of flip flops 718.1-718.m.

A selector 720 selects one of the SP1-SPm signals as the STOP signal based on
10 a combination of select signals S1-Sy. In some embodiments, selector 716 is a m:1 multiplexor.

A programming circuit 722 connects to selectors 716 and 718. Programming circuit 722 includes fuse devices, electrical fuse devices, laser fuse devices, storage elements, or other programmable elements. These elements are programmed to set a
15 combination of the SEL1-SELx and S1-Sy signals to select the START and STOP signals.

Figure 8 is a timing diagram for Figure 7. For clarity, Figure 8 shows only the ST1, ST2, ST3, and STn signals. The XCLK signal has a cycle time T_{CK} . The ST1 signal has a cycle time equaled to 2^1 times T_{CK} ($2 T_{CK}$). The ST2 signal has a cycle time
20 equaled to 2^2 times T_{CK} ($4 T_{CK}$). The ST3 signal has a cycle time equaled to 2^3 times T_{CK} ($8 T_{CK}$). The STn has a cycle time of 2^n times T_{CK} . In embodiments represented by Figure 8, the START signal is selected from the ST2 signal as an example. In other embodiments, the START signal can be selected from any one of the ST1-STn signals.

Figure 8 also shows only the SP1, SP2, and SPm signals for clarity. The SP1,
25 and SP2 signals are shifted from the START signal by one and two T_{CK} , respectively. The SPm signals are shifted from the START signal by mT_{CK} . In embodiments represented by Figure 8, the STOP signal is selected from the SP1 signal as an example. In other embodiments, the STOP signal can be selected from any one of the SP1-SPm signals.

Figure 9 shows memory device according to an embodiment of the invention. Memory device 900 includes a main memory 902 having plurality of memory cells arranged in rows and columns. The memory cells are grouped into a plurality of memory banks indicated by bank 0 through bank M (banks 0-M). Row decode 904 and
5 column decode 906 access the memory cells in response to address signals A0 through AX (A0-AX) on address lines (or address bus) 908. A data input path 914 and a data output path 916 transfer data between banks 0-M and data lines (or data bus) 910. Data lines 910 carry data signals DQ0 through DQN (DQ0-DQN). A memory controller 918 controls the modes of operations of memory device 900 based on control signals on
10 control lines 920. Examples of the control signals include a Chip Select signal CS*, a Row Access Strobe signal RAS*, a Column Access Strobe CAS* signal, a Write Enable signal WE*, and an external signal XCLK.

Memory device 900 further includes a delay locked circuit 905 for delaying the XCLK signal to generate an internal signal INTCLK. The INTCLK signal serves as a
15 clock signal to control a transfer of data on data output path 916. Delay locked circuit 905 periodically performs a measurement. The time interval between one measurement and the next measurement is unequal to the cycle time of the XCLK signal. Delay locked circuit 905 includes embodiments of delay locked circuit 100 (Figure 1 and Figure 3).

20 In some embodiments, memory device 900 is a dynamic random access memory (DRAM) device. In other embodiments, memory device 900 is a static random access memory (SRAM), or flash memory. Examples of DRAM devices include synchronous DRAM commonly referred to as SDRAM (synchronous dynamic random access memory), SDRAM II, SGRAM (synchronous graphics random access memory), DDR
25 SDRAM (double data rate SDRAM), DDR II SDRAM, and Synchlink or Rambus DRAMs. Those skilled in the art recognize that memory device 900 includes other elements, which are not shown for clarity.

Figure 10 shows a system 1000 according to an embodiment of the invention. System 1000 includes a first integrated circuit (IC) 1002 and a second IC 1004. IC 1002

and IC 1004 can include processors, controllers, memory devices, application specific integrated circuits, and other types of integrated circuits. In Figure 10, IC 1002 represents a processor and IC 1002 represents a memory device 1004. Processor 1002 and memory device 1004 communicate using address signals on lines 1008, data signals
5 on lines 1010, and control signals on lines 1020.

Memory device 1004 includes embodiments of memory device 900 (Figure 9) including delay locked circuit 905, which corresponds to delay locked circuit 100 (Figure 1 and Figure 3).

System 1000 includes computers (e.g., desktops, laptops, hand-helds, servers,
10 Web appliances, routers, etc.), wireless communication devices (e.g., cellular phones, cordless phones, pagers, personal digital assistants, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, camcorders, digital cameras, MP3 (Motion Picture Experts Group, Audio Layer 3) players, video games,
15 watches, etc.), and the like.

Although specific embodiments are described herein, those skilled in the art recognize that other embodiments may be substituted for the specific embodiments shown to achieve the same purpose. This application covers any adaptations or variations of the present invention. Therefore, the present invention is limited only by
20 the claims and all available equivalents.